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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,604	12/05/2001	Chad B. McBride	ROC920000324US1	3507

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EXAMINER	
LIOU, JONATHAN	

ART UNIT	PAPER NUMBER
2663	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,604	MCBRIDE ET AL.	
	Examiner	Art Unit	
	Jonathan Liou	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/05/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-10 and 12 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Pub. No. 2003/0067934 to Hooper et al.

3. As per claim 1, Hooper et al. teach a method to forward network data in a data processing system (**sec [0002], page 1**), comprising:

(a) receiving network data (**lines 2-4 in sec [0046], page 4**.)

(b) separating the network data into portions which will be modified and into portions which will not be modified; (**Hooper et al. teach the packet is comprised of one or more headers followed by a payload. The microengine**

(22a-22f, Fig.2) copies the payload portion of the packet to a packet buffer in DRAM (lines 4-7 in sec [0046], page 4.) Hence, the payload portion could be interpreted as a portion that will not be modified as claimed. Hooper et al. also teach changing of the header (lines 3-4, sec [0045], page 4) Hence; the header portion could be interpreted as a portion that will be modified as claimed.)

(c) storing both portions of the network data in a local memory; (**Hooper et al. teach the payload is sent to SDRAM (sec [0013].) The header portion could be sent through Fbus Interface to SDRAM (sec [0024] – sec [0025].)**

(d) forwarding the modifiable portions of the data to a cache associated with a processing element requesting at least the modifiable portion of the data; (**Hooper et al. teach forwarding the header portion of the packet data to a processor 20 in Fig. 1. They also teach that various parameters such as decap or encap flags of the header would also be send to the processor (sec [0046]-sec [0047], page 4.) Those flags could be interpreted as a processing element requesting as claimed. Hooper et al. also teach the cache is also included in the processor 20 in Fig. 2-2 (sec [0029], page 3.) Hence, header portions of the data forwards to a cache, since cache are located in the processor 20 as Hooper al taught.**)

(e) determining a destination of the modifiable portion; (**sec [0042]-sec [0043]**)

(f) modifying the modifiable portions within the requesting processing element; (**sec0046] – sec [0047]**)

(g) writing back the modified portion of the network data to the destination bypassing the local memory (**Hooper teach forwarding the header could have the microengine take the header and send it to the processor 20 or elsewhere, so that it can get reassembled with the payload (lines 12-17 in sec [0047], page 4.) Since Hooper teach the header portion is send to processor and do not teach the header portion would send through memory; therefor, the structure could be interpreted as bypassing the local memory as claimed.**)

4. As per claim 2, Hooper et al. teach the modifiable portion of the network data is a packet header of one network protocol which is modified to that of another network protocol (**sec [0045], page 4.**)

5. As per claims 3-6, Hooper et al. teach the network protocol could be ATM, Ethernet, PPP, or IP (**sec [0002], and sec [0033].**)

6. As per claim 7, Hooper et al. teach translating an address if the requesting processing element and the destination have different addresses of the local memory (**Hooper et al. teach extracting the packet headers and perform the destination protocol hashed lookup, which could be interpreted having the same function as comparing if the requesting processing element and the destination have different addresses as claimed (sec [0024].) Hooper et al. teach if the hash does not successfully resolve, the packet header is sent to the processor core 20 for additional processing (sec [0024].) the data could be direct memory access (sec [0025] – sec [0026].) Hooper et al. also teach the core processor access the microengines via the AMBA**

Translator. The AMBA translator performs an address translation between FBUS microengin transfer register locations and core processor addresses (sec [0028].))

7. As per claim 8, Hooper et al. teach the modification comprises updating an address to that of the destination (**Hooper et al. teach layer 2, 3, or 4 would read out the destination table and perform decap and encap operation of the header packet (sec [0033], sec [0043], and sec [0046].))**

8. As per claim 9, Hooper et al. teach the modification occurs in a network processor (**Hooper et al. teach the modification is done in the processor 12 in Fig. 1 and Fig. 3 (sec [0017], and sec [0030] – sec [0032].))**

9. As per claim 10, Hooper et al. teach the modification occurs in a local processing element (**the Table Managers 86 in the Control/management Processor 20 of Fig.4 could be interpreted as local processing element as claimed.**)

10. As per claim 12, Hooper teach an apparatus for data communication (**Fig.1-Fig.3.**) comprising:

(a) a network interface through which to receive incoming data comprised of at least one packet, the data packet having a modifiable portion and a portion that need not be modified (**Hooper et al. teach packets data enter though the network interface MAC devices (lines 2-5 in sec [0030], page 3.) The same basis and rational for claim rejections as applied to claims 1 (a), (b) are applied to the remainder of claim 12 (a).**)

(b) a local memory connected to the network interface (**Fig.1 shows SDRAM is connected to the network processor 12.**), the local memory for receiving the data and storing the modifiable portion from the portion that need not be modified; (**the same rationale as applied to claim 1 (c) are applied.**)

(c) a modifier which updates the modifiable portion of the data packet; (**Hooper et al. teach a process fro encapsulating/decapsulating generic protocols to perform the header changes. This could be interpreted as a modifier as claimed. This process provides the function of updating the header of the data packet (sec [0045] – sec [0047].**)

(d) a bus interface; (**line 5, sec [0013]**)

(e) an interconnect fabric connected to the bus interface by which to forward the modifiable portion and the portion of the data that need not be modified to its destination (**Hooper et al. teach microengines connected to the bus interface. The microengines could be interpreted as an interconnect fabric as claimed. The microengines also perform forward the header portion and payload portion to its destination (sec [0013], sec [0046] – sec [0047].**))

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which

said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0067934 to Hooper et al. as applied to claim 1 above, and further in view of U.S. Pat. No. 6,754,662 to Li.

13. As per claim 11, Hooper et al. teach the method of claim 1, wherein the modification occurs in an embedded processor (**Fig.1 and Fig.3, Hooper et al.**). He does not specifically teach using an application specific integrated circuit, ASIC, to function the modifications method of his structure. Nevertheless, Li teach the hash-cashing packet classification approach to appropriate classifies the packets, and this method could be done by programmable logic architectures such as ASICs (**col 3, lines 35-49, Li.**) Hooper et al. teach the same method for the structure of changing the header of the packet (**sec [0024], Hooper et al.**) Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have modification function in an embedded processor by using ASICs because it would provide the program logic circuit to perform necessary functions for modification. In addition, ASICs is broadly used in the routing system and Hooper et al. does teach to performs a microprogrammable hashed lookup (**sec [0024], Hooper et al.**)

14. Claims 13-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Pub. No. 2003/0067934 to Hooper et al. as applied to claim 12 above, and further in view of U.S. Pub. No. 2002/0027901 to Liu et al.

15. As per claims 13-14, Hooper et al. teach the apparatus of claim 12. Hooper et al. does not specify what types of incoming data could be.

Nevertheless, Liu et al. teach Network interfaces could receive various signals. The interfaces typically handle one or more data types, including, as examples, analog, digital, broadband, wireless, and optical data.

It is obvious for one who have ordinary skill in the art to understand a network interface would be possible to receive the incoming data with different type of signal, such as analog, digital, or optical data. In addition, Liu et al. teach the networks enable the packets of a particular transmission to travel from source to destination, which would be related to the field of data transfer in a data processing system. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to receive incoming data that is digital, analog, or optical data based on Hooper et al.'s structure in view of Liu et al. because this would give the plurality of types of input signals to the network interfaces for forwarding data. In addition, Hooper et al. teach incoming data could have ATM, Ethernet and other types of packets enter through the network interface (**sec [0030].**)

16. As per claim 15, Hopper et al. disclosed the structure would perform the same function as a memory bypass mechanism as claimed (**Hooper teach forwarding the header can have the microengine take the header and send it to the processor 20 or elsewhere, so that it can get reassembled with the payload (lines 12-17 in sec [0047], page 4, Hooper et al.), and Hooper et al. teach the apparatus of their structure through Fig. 1 to Fig. 3.**) The mechanism comprising:

the same basis and rational as applied to claims 12-14 above are applied the remainder of the claim 15.

17. As per claim 16, Hooper et al. teach the modifiable portion of the received data is a header stating a network protocol of the data or a destination address of the received data (**Hooper et al. teach the received data is a header portion stating a network protocol of the data. (Sec [0045], Hooper et al.)**)

18. As per claim 17, Hooper et al. teach the received header is of a first network protocol and the modified header is of a second network protocol (**Hooper et al. teach a example by taking out the first network protocol, IP header, and adding the second network protocol, ATM network (sec [0051], Hooper et al.**)

19. As per claim 18, Hooper et al. teach the first and second network protocols are selected from the group consisting of: asynchronous transfer mode, Ethernet, Internet protocol, and Point-to-Point protocol. (**Hooper et al. teach the network protocol could be selected from ATM, Ethernet, PPP, or IP (sec [0002], and sec [0033], Hooper et al.)**)

20. As per claim 19, Hooper et al. teach the modifying means is a processing element in a network processor (**Fig. 3, Hooper et al.**)

21. As per claims 20-21, Hooper et al. teach the destination is a different processing element in the network processor, and the destination is a second memory (**Hooper et al. tech the packet Buffer could be the destination of the packet and stored in the DRAM, which is different from the network processor as shown in Fig.4 (Fig. 4 and sec [0033], Hooper et al.)**)

Hooper et al. teach means to receive incoming data (**lines 2-4 in sec [0046], Hooper et al.**), means to separate the received data into a modifiable portion and a non-modifiable portion (**the same rationale as applied to claim 1(b) are applied.**), means to store the received data in a first memory (**the same rationale as applied to claim 1(c) are applied.**), means to forward the modifiable portion of the data to a modifying means (**sec [0046] –sec [0047], Hooper et al.**), means to forward the non-modified portion to a destination (**Hooper et al. teach the microengine copied the payload portion of the packet to a packet buffer in DRAM and it would reassemble with the header by processor (sec [0046]-sec [0047], Hooper et al.) The payload portion could be interpreted as non-modified portion as claimed.**), means to modify the modifiable portion (**sec [0046] – sec [0047], Hooper et al.**), means to forward the modified portion of data directly to its destination bypassing storing the modified portion in the first memory (**Hooper et al. teach forwarding the header to processor. Since they do not teach the header portion go through the local memory system, the header portion could directly to the processor as the destination to reassemble with the payload; hence, this could be interpreted as bypassing storing the modified portion in the SDRAM, which could be the first memory as claimed.**)

Hooper et al. do not teach receiving optical and/or digital data as claimed. Nevertheless, Liu et al. teach Network interfaces could receive optical or digital data as taught in the claim rejections 13-14 above in the office action. Therefore,

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jonathan Liou whose telephone number is 571-272-8136. The examiner can normally be reached on 8:00AM ~ 5:00PM Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ricky Ngo can be reached on 571-272-3139. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jonathan Liou

08/22/2005

RICKY NGO
PRIMARY EXAMINER
8/29/05